TT-CW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Shay Ben-David, et al.

Docket No.: IL920030035US1

Serial No.: 10/695,970

Examiner:

Filed: October 29, 2003

Group Art Unit: 2183

For: Vectorization in a SIMdD DSP Architecture

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATE OF MAILING UNDER 37 CFR 1.8(a)

I hereby certify that the attached correspondence comprising:

1. Information Disclosure Statement Transmittal Letter;
2. PTO Form 1449 with 16 references attached
3. Return Postcard

is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on December 1, 2005.

Jeanne M. Jordan

(Type or print name of person mailing paper)

Jeanne M. Jordan

(Signature of person mailing paper)

In re Patent Application of: Shay Ben-David, et al. : **Confirmation No.:** 7994

Serial No.: 10/695,970 : **Group Art Unit:** **2183**

Filed: October 29, 2003 : **Examiner:**

: **Date:** December 1, 2005

For: **Vectorization in a SIMdD DSP Architecture**

INFORMATION DISCLOSURE STATEMENT under 37 C.F.R. 1.97(b)(3)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Listed on form PTO-1449 are a number of documents which may be material to the examination of the above-referenced application. It is respectfully requested that the Examiner consider each of the cited documents and return an initialed copy of the form PTO-1449.

In accordance with 37 CFR 1.97(b), this information disclosure statement is being filed within three months of the filing date of the application or before the mailing date of the first Office Action on the merits, which ever event occurs last. **Please charge any fee necessary to enter this paper to deposit account 09-0468.**

Respectfully submitted,
Attorney for the Applicant(s)

By: Stephen C. Kaufman
Registration No.: 29,551

IBM Corporation
Intellectual Property Law Department
P. O. Box 218
Yorktown Heights, N. Y. 10598
Telephone No.: (914) 945-3197
Fax No.: (914) 945-3281

IBM Docket: IL920030035US1

FORM PTO-1449 (Modified)	ATTY. DOCKET NO.	SERIAL NO.:
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	IL920030035US1	10/695,970
	APPLICANT: Ben-David et al.	
	FILING DATE: 29-Oct-2003	GROUP: 2183

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA	**6665790**		Glossner et al.			2000-02-29
	AB	**6915411**		Moreno et al.			2002-07-18
	AC	**2004-0078554**		Glossner et al.			2003-06-07

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AD	Preeti Ranjan Panda, Nikil D. Dutt, and Alexandru Nicolau. "Efficient utilization of sratch-pad memory in embedded processor applications", in European Design and Test Conf., March 1997
	AE	Keith D. Cooper, Timothy J. Harvey. "Compiler controlled Memory", Eighth Int. Conf. on Architectural Support for Programming Languages and Operating Systems, pp. 100-104, Oct, 1998
	AF	Masaaki Kondo, Hideki Okawara, Hiroshi Nakamaru, Taisuke Boku. "SCIMA: Software Controlled Integrated Memory Architecture for High Performance Computing", http://citeseer.nj.nec.com/376639.html
	AG	William Y. Chen, Roger Bringmann, Scott A Mahlke, Richard E. Hank, James E. Sicolo. "An Efficient Architecture for Loop Based Data Preloading", 25th Annual International Symposium on Microarchitecture (1992) http://citeseer.nj.nec.com/chen92efficient.html
	AH	Matthew A. Postiff, Trevor Mudge. "Smart Register Files for High Performance Microprocessors". http://citeseer.nj.nec.com/postiff99smart.html
	AI	Matthew A. Postiff, David Greene, Steve Raasch, Trevor Mudge. "Integrating Superscalar Processor Components to Implement Register Caching". http://citeseer.nj.nec.com/468226.html
	AJ	Jesus Corbal, Roger Espasa, and Mateo Valero. "Exploiting a new level of DLP in multimedia applications", in Intl. Symposium on Microarchitecture, pages 72-79, 1999.

EXAMINER□ DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. IL920030035US1	SERIAL NO.: 10/695,970
	APPLICANT: Ben-David et al.	
	FILING DATE: 29-Oct-2003	GROUP: 2183

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AK	Huy Nguyen and Lizy Kurian John. "Exploiting SIMD parallelism in DSP and multimedia algorithms using the AltiVec technology", in Intl. Conf. on Supercomputing, pages 11-20 1997
	AL	A. J. C. Bik, M. Girkar, P. M. Grey, and X. Tian. "Efficient exploitation of parallelism on Pentium III and Pentium 4 processor-based systems", Intel Technology J., February 2001.
	AM	Andreas Krall and Sylvain Lelait. "Compilation techniques for mutimedia processors", Intl. J. of Parallel Programming, 28(4):347-361, 2000.
	AN	Samuel Larsen, Emmet Witchel, and Saman Amarasinghe. "Techniques for increasing and detecting memory alignment", Technical Memo 621, MIT LCS, Novermber 2001.
	AO	David Callahan et al. "Improving Register Allocation for Subscripted Variables", Proceedings of the ACM SIGPLAN '90 Conference on Programming Language Design and Implementation, White Plains NY, June 20-22, 1990.
	AP	Kandemir et al., "Optimizing Inter-Nest Data Locality", CASES 2002, Oct. 8-11 2002, Grenoble, France
	AQ	Doshi et al., "Optimizing Software Data Prefetches with Rotating Registers", IEEE 2001, 257-267.

EXAMINER□ DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. IL920030035US1	SERIAL NO.: 10/695,970
	APPLICANT: Ben-David et al.	
	FILING DATE: 29-Oct-2003	GROUP: 2183

REFERENCE DESIGNATION **U.S. PATENT DOCUMENTS**

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	Jaewook Shin et al., "Compiler-Controlled Caching in Superword Register Files for Multimedia Extension Architectures", in Int. Conf. on Parallel Architectures and Compiler Techniques, pages 45--55, 2002.
	AS	Keith Cooper et al., "Cross-loop Reuse Analysis and its Application to Cache Optimizations", Lecture Notes In Computer Science; Vol. 1239 archive Proceedings of the 9th International Workshop on Languages and Compilers for Parallel Computing, Pages: 1-19, 1996

EXAMINER□	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.